International Journal of Electronics Communication and Computer Engineering
Volume 8, Issue 4, ISSN (Online): 2249–071X

Reducing Power and Leakage in CMOS Logic with Sleep and Stack Transistor Technique

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Date of publication (dd/mm/yyyy): 12/08/2017

Abstract **– The major design constraint for VLSI circuits and systems is the reduce power dissipation. The power dissipation in VLSI circuits depends on the switching activity, supply voltage and output load capacitance. The leakage power dissipation cause by parasitic pn junctions and subthreshold leakage is a component of static power dissipation in CMOS circuits. It is because of the generation of leakage currents in the MOS transistors. The various methodologies such as series connected stack transistors, sleep transistor, sleepy keeper transistors techniques. These techniques reduces the static power with a moderate area overhead as compare to CMOS circuit design.**

The main benefit of using stack and sleep transistor technique is that it keeps the logic state and also lowers the subthreshold leakage power dissipation. It has been shown before that the series connection of two half size off transistors has considerably reduced sub-threshold leakage as compared to a one off transistor. In stack transistor technique two half channel width transistors are connected in series to for one of the transistor in pull up and pull down networks with gates to increase the stack effect, it will increase the resistance between the supply and ground. Therefore, the leakage of the logic gate is reduced. A MOS transistor in the circuit is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the subthreshold leakage power. However, increase in the number of transistors increases the overall propagation delay of the circuit.

The simulation results shows that the power dissipation of basic CMOS circuit is 1.194uW whereas the power dissipation of precharge evaluate logic base sleep transistor is 0.264uW and for stack transistor method it is at 0.491uW. The sleep transistor reduces the leakage power by disconnection the CMOS logic from its power supply rail when it is in standing mode while the stack transistor reduces the power dissipation by cascading transistor.

Keywords **– Stack Transistor, Sleep Transistor, Precharge Evaluate, Leakage Power.**

I. INTRODUCTION

The variation in subthreshold leakage power increases the static power dissipation in CMOS circuits. The leakage power dissipation is mainly due to the subthreshold leakege and reversly biased pn junction when the transistor is at standing mode. The subthreshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to source voltages below the threshold voltage. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases which increases the sub-threshold leakage power.

II. LEAKAGE POWER

The main advantage of CMOS logic family use in VLSI circuit design is its lowest power consumption. But as the transistor size reduces with technology scale down the drain punch through and body effect alters the performance of transistor. One of the main contributor for the static power dissipation is sub threshold leakage current which is shown in the Figure 2 i.e., the drain to source current when the gate voltage is smaller than the threshold voltage. As the technology feature size shrink sub current is increases exponentially as the decrease of threshold voltage.

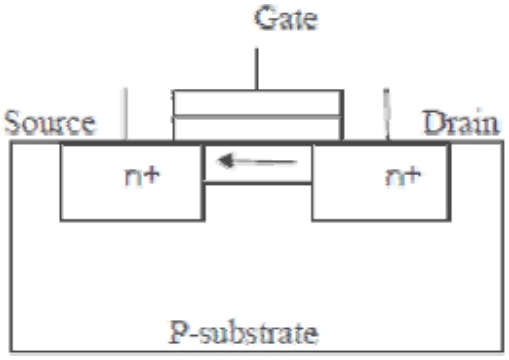

Fig. 1. A: Sub-threshold Leakage of an NMOS

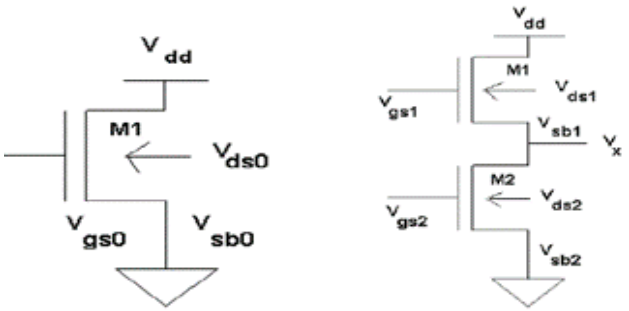

Fig. 1. B: (i) Single Transistor (ii) Stacked transistor

Stacking transistor can reduce sub-threshold leakage. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power.

Leakage Power Source

Subthreshold leakage current is the most dominant component of leakage current (power) in short channel

MOS transistors. This leakage current is caused by the inability to completely turn off a MOS transistor. Due to the reversly biased pn junction the transistor conducts even in weak inversion region below the threshold voltage of the MOS transistor.

There are four main sources of leakage current in a CMOS transistor:

1. Junction Leakage(I1): The junction leakage occurs from the source or drain to the substrate through the reversebiased diodes when a transistor is OFF. A reverse-biased pn junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction.
2. Gate-Induced Drain Leakage(I3): The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at VDD, significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current.
3. Gate Direct Tunneling Leakage(I2): This current results from the tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. This direct tunneling current increases exponentially with the gate oxide thickness and supply voltage.
4. Subthreshold Leakage(I4): The subthreshold leakage is the drain-source current of a transistor I.e channel punch through current.

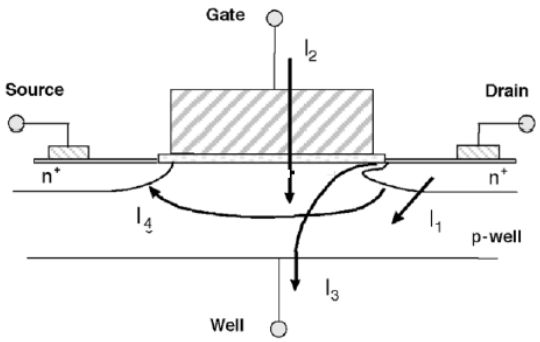

Fig. 2. Leakage currents in MOSFET

Increasing the threshold voltage of a transistor reduces the leakage current exponentially, but it has a marginal effect on the dynamic power dissipation. On the other hand, reducing the width of a transistor reduces both leakage and dynamic power, but at a linear rate only.

2. Stack technique

In this technique NMOS and PMOS transistors can be added in series with gates to increase the stack effect, it will increase the resistance between the supply and ground. Therefore, the leakage of the logic gate is reduced. A MOS transistor in the circuit is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the subthreshold leakage power. However, increase in the number of transistors increases the overall propagation delay of the circuit. When a stack of two or more transistors are turned off, the time required for voltages and currents to settle to quiescent levels is large and can vary over a wide range.

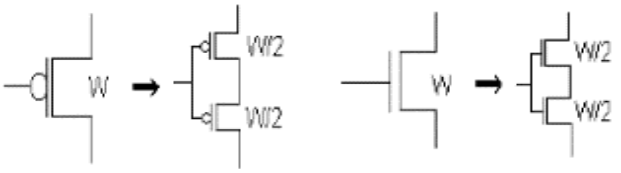

Fig. 3. Stack Technique series connected half channel width MOSFET

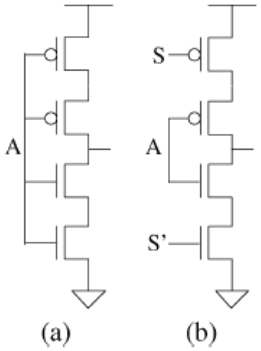

Fig. 4. Fig Not logic Gate using (a) stack method (b) Sleep transistor method

3. *Sleep Technique*

Sleep transistors of high threshold voltages are used in the Sleep technique. A sleep pMOS transistor is placed between the supply voltage, VDD and the pullup network and a sleep nMOS transistor is placed between the pulldown network and the ground, GND. These sleep transistors are turned ON when the circuit is in active state and turned OFF when the circuit is in sleep state. This technique reduces the subthreshold leakage current by cutting off the logic circuitry from the power supply voltage and ground in the sleep state. These sleep transistors are driven by sleep signals. Using this technique the present state of the circuit is lost and thus results in destruction of the present logic state.

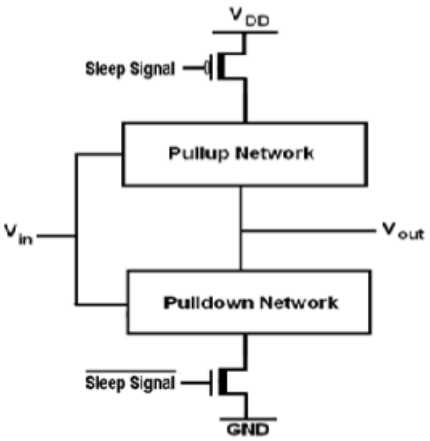

Fig. 5. Sleep transistor technique

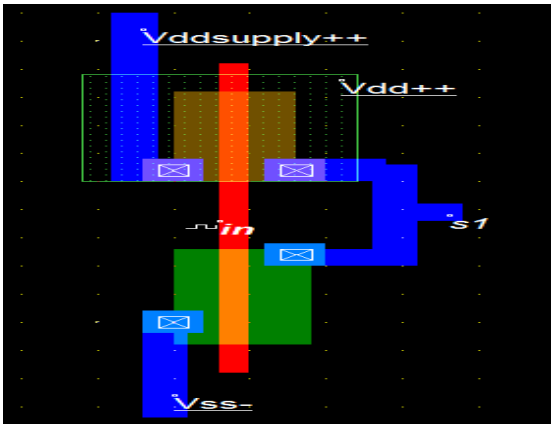

Fig. CMOS Inverter Logic

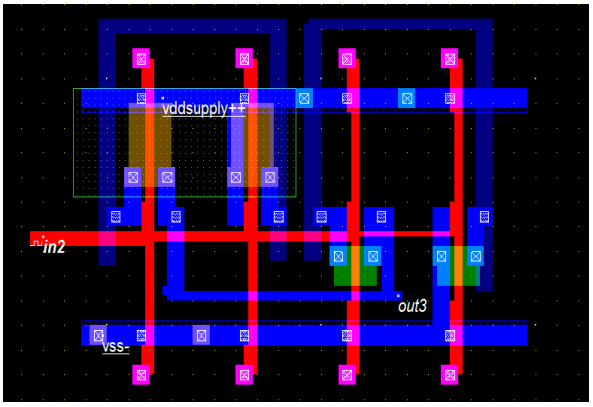

Fig. CMOS Inverter Logic with stack Transistor

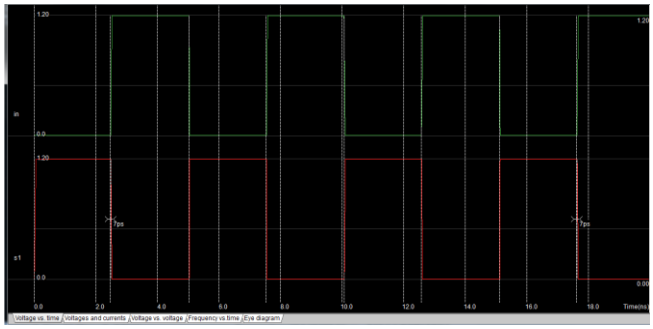
Fig. Timing Simulation of CMOS Inverter Logic

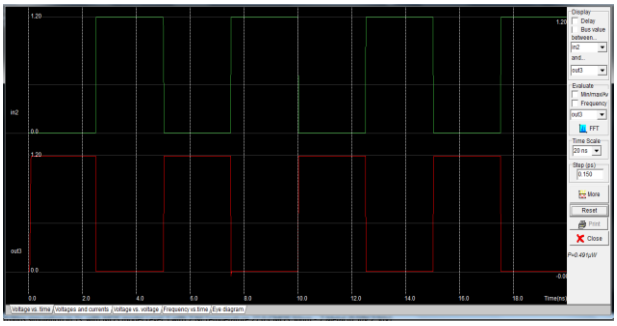
Fig. Timing simulation of CMOS Inverter Logic with stack Transistor

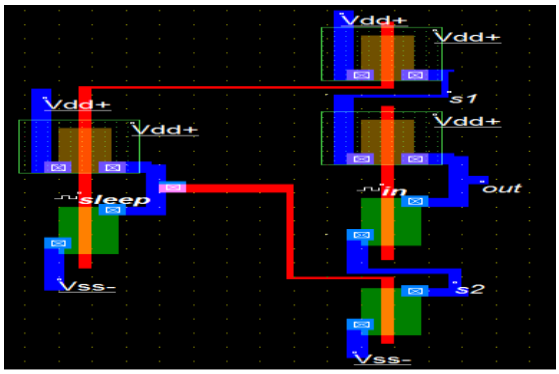

Fig. CMOS Layout of Inverter logic with precharge and evaluate logic transistor

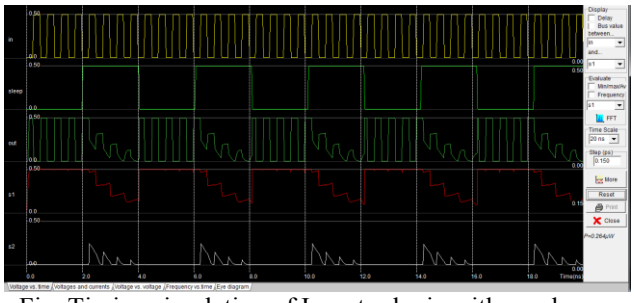
Fig. Timing simulation of Inverter logic with precharge and evaluate logic transistor.

Result Analysis:

Table 1: Parametric Analysis of CMOS Inverter Logic.

CMOS Logic Design Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
Inverter	0 1	1 0	2	0.28fF	1.194uW	0.002ns

Table 2: Parametric Analysis of CMOS AND Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
AND	00 01 10 11	0 0 0 1	6	0.15fF	7.2uW	0.002/0.001ns

Table 3: Parametric Analysis of CMOS Adder Logic.

Module	No. of T	Ouput Load	Power Dissipation	Area (um^2)	Delay
Adder	46	0.15fF	1.217 uW	40.375	0.002/0.001ns

CMOS Layout Design with Precharge Evaluate Logic (Sleep TransistorMethod).

Table 4: Parametric Analysis of Sleep Transistor Inverter Logic.

Module	No. of T	Ouput Load	Power Dissipation	Area (um^2)	Delay
Sleep Transistor Inverter	4	0.28fF	0.264 uW	4.875	0.002/0.001ns

Table 5: Parametric Analysis of Sleep Transistor NAND Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
Sleep Transistor NAND	00 01 10 11	1 1 1 0	8	0.43fF	1.46 uW	0.001/0.001ns

Table 6: Parametric Analysis of CMOS Flip Flop Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
Flip Flop	0 1	0 1	14	0.55fF	31.83 uW	0.0014/0.001ns

Stack Transistor Logic:

Table 7: Parametric Analysis of Stack Transistor Inverter Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
Stack Transistor Inverter	0 1	1 0	4	0.44fF	0.491uW	0.003/0.001ns

Table 8: Parametric Analysis of Stack Transistor NAND Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Area (um^2)	Delay
Stack NAND	00 01 10 11	1 1 1 0	8	0.5fF	0.966uW	1.828	0.004/0.002ns

Table 9: Parametric Analysis of Stack Transistor Adder Logic.

Module	No. of T	Ouput Load	Power Dissipation	Area (um^2)	Delay
Stack transistor Adder	58	0.15fF	1.259 uW	80	0.002/0.001ns

Table 10: Parametric Analysis of CMOS Flip Flop Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
Flip Flop	0 1	0 1	16	0.55fF	33 uW	0.0014/0.001ns

Table 11: Parametric Analysis of Flip Flop with Threshold Voltage Logic.

Module	D in	Q Out	No. of T	Ouput Load	Power Dissipation	Delay
Threshold Flip Flop (Body Bias)	0 1	0 1	15	0.54fF	0.710 uW	0.0010/0.001ns

III. Conclusion

This work reviewed circuit optimization design techniques for controlling the OFF current of CMOS circuits in both standby and active modes of circuit operation. The subthreshold leakage control techniques that do not adversely affect the circuit performance and layout cost. This is especially important in light of both statistical process parameter variations and their impact on leakage currents. The simulation results shows that the power dissipation of basic CMOS circuit is 1.194uW whereas the power dissipation of precharge evaluate logic base sleep transistor is 0.264uW and for stack transistor method it is at 0.491uW. The sleep transistor reduces the leakage power by disconnection the CMOS logic from its power supply rail when it is in standing mode while the stack transistor reduces the power dissipation by cascading transistor.

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